

CLAIMS

What is claimed is:

- 1 1. A computer system comprising:
2 a bus; and
3 a chipset, coupled to the bus, to detect the slew rate of a signal transmitted
4 over the bus via the chipset, and to adjust the slew rate based upon the state of
5 the signal.
- 1 2. The computer system of claim 1 wherein the chipset comprises:
2 a slew rate detection mechanism to detect the slew rate and generate a
3 signal to indicate the status of the slew rate; and
4 control logic, coupled to the slew rate detection mechanism, to receive the
5 signal and modify the slew rate based upon the signal.
- 1 3. The computer system of claim 1 wherein the chipset further comprises an
2 input/output (I/O) buffer coupled to the control logic.
- 1 4. The computer system of claim 2 wherein the control logic reduces the slew
2 rate if the signal received from the slew rate detection mechanism indicates that
3 the slew rate is too fast.
- 1 5. The computer system of claim 2 wherein the control logic increases the
2 slew rate if the signal received from the slew rate detection mechanism indicates

3 that the slew rate is too slow.

1 6. The computer system of claim 2 wherein the slew rate detection
2 mechanism includes a capacitor, coupled to the bus, to integrate the received
3 signal current.

1 7. The computer system of claim 6 wherein the slew rate detection
2 mechanism further includes:
3 a reference current generator to generate a reference current; and
4 a comparator to compare the received signal current to the reference
5 current.

1 8. The computer system of claim 7 wherein the slew rate detection
2 mechanism further includes:
3 a first converter, coupled to the capacitor and the comparator to convert
4 the signal current to a signal voltage; and
5 a second converter, coupled to the reference current generator and the
6 comparator to convert the reference to a reference voltage.

1 9. The computer system of claim 6 wherein the comparator is an operational
2 amplifier.

1 10. The computer system of claim 1 wherein the bus is a high-speed bus.

1 11. A computer system comprising:
2 a main memory device;
3 a memory bus coupled to the main memory device; and
4 a memory controller, coupled to the bus, to detect the slew rate of a signal
5 transmitted over the bus via the chipset, and to adjust the slew rate based upon
6 the state of the signal.

1 12. The computer system of claim 11 wherein the memory controller
2 comprises:
3 a slew rate detection mechanism to detect the slew rate and generate a
4 signal to indicate the status of the slew rate; and
5 control logic, coupled to the slew rate detection mechanism, to receive the
6 signal and modify the slew rate based upon the signal.

1 13. The computer system of claim 12 wherein the control logic reduces the
2 slew rate if the signal received from the slew rate detection mechanism indicates
3 that the slew rate is too fast.

1 14. The computer system of claim 12 wherein the control logic increases the
2 slew rate if the signal received from the slew rate detection mechanism indicates
3 that the slew rate is too slow.

1 15. The computer system of claim 12 wherein the slew rate detection
2 mechanism includes a capacitor, coupled to the bus, to integrate the received
3 signal current.

1 16. The computer system of claim 15 wherein the slew rate detection
2 mechanism further includes:
3 a reference current generator to generate a reference current; and
4 a comparator to compare the received signal current to the reference
5 current.

1 17. The computer system of claim 16 wherein the slew rate detection
2 mechanism further includes:
3 a first converter, coupled to the capacitor and the comparator to convert
4 the signal current to a signal voltage; and
5 a second converter, coupled to the reference current generator and the
6 comparator to convert the reference to a reference voltage.

1 18. A method comprising:
2 transmitting a signal from an input/output (I/O) buffer within a chipset
3 over a bus;
4 receiving the signal at a slew rate detection mechanism within the chipset
5 via the bus;

6 generating a signal indicating the status of the slew rate; and
7 adjusting the slew rate at control logic within the chipset based upon the
8 signal.

1 19. The method of claim 18 further comprising generating a reference current
2 at the chipset.

1 20. The method of claim 19 further comprising:
2 converting the signal current to a signal voltage;
3 converting the reference current to a reference voltage; and
4 comparing the reference voltage to the signal voltage.

21. The method of claim 18 wherein adjusting the slew rate comprises
modifying the amplification of a second signal at the I/O buffer.

22. An apparatus comprising:
a slew rate detection mechanism to detect the slew rate of a signal
transmitted over a bus via the memory controller, and to adjust the slew rate
based upon the state of the signal; and
detect the slew rate and generate a signal to indicate the status of the slew
rate bus

1 23. The apparatus of claim 22 wherein the slew rate detection mechanism
2 generates a signal to indicate the status of the slew rate bus

1 24. The apparatus of claim 23 further comprising control logic, coupled to the
2 slew rate detection mechanism, to receive the signal and modify the slew rate
3 based upon the signal.

1 25. The apparatus of claim 24 further comprising an input/output (I/O)
2 buffer coupled to the control logic.

1 26. The apparatus of claim 22 wherein the slew rate detection mechanism
2 includes a capacitor, coupled to the bus, to integrate the received signal current.

1 27. The apparatus of claim 26 wherein the slew rate detection mechanism
2 further includes:

3 a reference current generator to generate a reference current; and

4 a comparator to compare the received signal current to the reference
5 current.

1 28. The apparatus of claim 27 wherein the slew rate detection mechanism
2 further includes:

3 a first converter, coupled to the capacitor and the comparator to convert
4 the signal current to a signal voltage; and

5 a second converter, coupled to the reference current generator and the
6 comparator to convert the reference to a reference voltage.